THERMAL PERFORMANCE AND KEY CHALLENGES FOR FUTURE CPU COOLING TECHNOLOGIES

Ioan Sauciuc, Ravi Prasher, Je-Young Chang, Hakan Erturk, Gregory Chrysler, Chia-Pin Chiu, Ravi Mahajan

Intel Corporation
5000 W. Chandler Blvd., Chandler, AZ, USA, 85226
ioan.sauciuc@intel.com

ABSTRACT
Over the past few years, thermal design for cooling microprocessors has become increasingly challenging mainly because of an increase in both average power density and local power density, commonly referred to as “hot spots”. The current air cooling technologies present diminishing returns, thus it is strategically important for the microelectronics industry to establish the research and development focus for future non-air cooling technologies.

This paper presents the thermal performance capability for enabling and package based cooling technologies using a range of “reasonable” boundary conditions. In the enabling area a few key main building blocks are considered: air cooling, high conductivity materials, liquid cooling (single and two-phase), thermoelectric modules integrated with heat pipes/vapor chambers, refrigeration based devices and the thermal interface materials performance. For package based technologies we present only the microchannel building block (cold plate in contact with the back-side of the die). It will be shown that as the hot spot density factor increases, package based cooling technologies should be considered for more significant cooling improvements.

In addition to thermal performance, a summary of the key technical challenges are presented in the paper.

NOMENCLATURE
A Area (m²)
COP coefficient of thermal performance
CFD Computational Fluid Dynamics
cp specific heat (J/kg-K)
DFjc Density factor from junction to case (1/cm²)
Dh hydrodynamic diameter of the channel (m)
harea equivalent heat transfer coefficient of the fins based on heat sink base area (W/ m²°C)

HX remote heat exchanger

\( \bar{h} \) average heat transfer coefficient (W/ m²°C)
k thermal conductivity (W/m-K)
m mass flow rate (kg/s)
NuDn Nusselt number for the rectangular channel subject to constant heat flux boundary condition
Q power (W)
Rjc Normalized Thermal Impedance from junction to case (°C-cm²/W)
T temperature (°C)
Ta Ambient temperature local to the heat sink (°C)
Tc Package case temperature (°C)
TDP Thermal Design Power (W)
TIM Thermal Interface Material impedance (°C cm² /W)
Tj Junction or die temperature (°C)
Tj,max Junction temperature at the hottest point of the die (°C)
Ts Heat sink temperature (°C)
Tx Temperature at any location on the thermal solution (°C)
ZT Thermoelectric Figure of Merit

Greek symbols

\( \eta \) fin efficiency
\( \Psi_{cs} \) Thermal Resistance from case to sink (°C/W)
\( \Psi_{jc} \) Thermal Resistance from junction to case (°C/W)
\( \Psi_{js} \) Thermal Resistance from junction to sink (°C/W)
\( \Psi_{sa} \) Thermal Resistance from sink to ambient (°C/W)
\( \psi_{x,y} \) thermal resistance (°C/W) between point x and y at non-uniform heat flux
\( \theta_{x,y} \) thermal resistance (°C/W) between point x and y at uniform heat flux

Subscripts
The cooling device. The "Spreading" building block refers to improvements in the interaction between the ambient air and the "Spreading" building blocks. The "Air Side Forced Convection" blocks are considered: the "Air Side Forced Convection" and on the main heat transfer function. Thus, two major building blocks are considered.

One classification for the CPU cooling technologies depends on the area of the application. Thus from the chip manufacturer point of view, the cooling technologies are classified as: package based (included by the package manufacturer) and enabling (usually added on top of the package by the Original Equipment Manufacturers – OEMs–). As most researchers will agree, the further away the cooling device is located from the hot spot the less contribution it has to the total thermal stack up has. This paper will show that as the hot spot density increases, package based cooling technologies should be considered to accommodate future CPU requirements.

The authors consider that the “Spreading” building block is the most promising for future improvements of the overall thermal cooling solutions. For the “Spreading” Building Block this paper classifies the main technologies in two main sub-categories:

(A) Technologies which increase the “effective” thermal conductivity for materials or devices compared to conventional designs. This category includes thermal interface materials, diamond, graphite materials and vapor chambers/heat pipes spreaders. Also technologies which help to spread the heat to a large remote heat exchanger (i.e. single or two-phase liquid cooling) are included here.

(B) Refrigeration Technologies (i.e. thermoelectric or vapor compression refrigeration).

In the enabling area a few key main technologies are considered and they will be discussed: liquid cooling (single and two-phase), thermoelectric integrated with heat pipes/vapor chambers, and refrigeration based devices. For the package based technologies, we will focus on the performance of the single phase micro channel based device, since this looks most promising to further improve cooling. This is because it eliminates several interfaces and provides the ability of having a large remote heat exchanger.

By using the density factor metric, this paper will show that at high hot spots densities the cooling technologies need to merge in a total single solution combining both the package and the enabling cooling solutions. At lower hot spot densities some enabling technologies may have better advantages. However, most of these technology options present some high risk items and key challenges which are not solved as of today. It is expected that the present work will significantly help the industry to focus their research in addressing these challenges and improve the return on investment.

Also, this paper addresses and summarizes the cooling capability of most promising technologies and determines their contribution to the total thermal resistance, all within a...
reasonable range of boundary condition encountered in CPU cooling.

DEFINITIONS AND METRICS

Thermal Resistance Definition

There are two major CPU architectures today No-Lidded-(Architecture I- Figure 1) and Lidded(Architecture II- Figure 2).

\[
\Psi_{x,y} = \frac{T_x - T_y}{TDP}, \quad (1)
\]

Where x and y can represent different points on the solution for Architecture II. In other words it is a measure of the resistance to heat flow between the two specified points. The most used resistances in electronic cooling are \(\Psi_{j,a}\) (junction-to-ambient), \(\Psi_{c,a}\) (case-to-ambient) and \(\Psi_{s,a}\) (sink-to-ambient or heat sink resistance). A typical Architecture II test vehicle may have a 30 mm x 30mm heat spreader attached to a 10 mm x 10 mm die.

Density Factor Definition

In addition to the above metrics, Torresola et. al [21] have proposed the density factor (DF) definition as a significant metric in understanding the cooling capability for different thermal solutions used in CPU cooling. This metric can be used to quantify the impact of non-uniform die heating (so called “hot spots”) on thermal management difficulty. The advantage of using this metric is its ability to provide a better “apples-to-apples” comparison of the impact of different power maps and die sizes on thermal management. The junction-to-case Density Factor (DF\(_j\)) parameter can be used to quantify the impact of die size and die power maps on the thermal resistance. In this case, the junction temperature (\(T_j\)) and the case temperature (\(T_c\)) are the most convenient temperatures to use. This simple metric is defined as the ratio of thermal resistance to thermal impedance.

Thus the junction-to-case density factor is defined as:

\[
DF_{jc} \equiv \frac{\Psi_{j,c}}{R_{j,c}} \quad (2)
\]

Thermal impedance, \(R_{j,c}\), is defined as the thermal resistance normalized by die area when the die is uniformly powered.

COOLING BUILDING BLOCKS

Air Side Cooling Building Block

This section is focusing on determining the focus parameters for air cooling extensions. For this building block the most common metric used to compare the thermal performance of heat sinks is the sink to ambient thermal resistance as defined by Equation (2), \(\Psi_{s,a}\) (sink-to-ambient or heat sink resistance).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Resistance Variation [deg.C/W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heat Source edge [mm] (10, 30)</td>
<td>-0.08</td>
</tr>
<tr>
<td>Footprint edge [mm] (50, 100)</td>
<td>-0.059</td>
</tr>
<tr>
<td>Base Conductivity [W/mK] (180, 390)</td>
<td>-0.048</td>
</tr>
<tr>
<td>Fin Gap [mm] (0.9, 1.6)</td>
<td>0.036</td>
</tr>
<tr>
<td>Total Height [mm] (40, 80)</td>
<td>-0.026</td>
</tr>
<tr>
<td>Velocity between plates [m/s] (3, 6)</td>
<td>-0.016</td>
</tr>
<tr>
<td>Base Thickness [mm] (4, 10)</td>
<td>-0.016</td>
</tr>
<tr>
<td>Fin conductivity [W/mK] (180, 390)</td>
<td>-0.015</td>
</tr>
</tbody>
</table>

Sauciuc et al. [10] presented a summary of statistical Design of Experiments (DOE) used to determine how to best minimize the sink to ambient thermal resistance [Figure 3]. The parameters used are self explanatory with their range of variation listed between the brackets. The vertical pareto chart presented in Figure 3 shows the magnitude of the parameter influence. The values showing the resistance variation show the average thermal resistance reduction over the range of boundary conditions considered. It can be seen that the major focus areas to extend air cooling are: increase the heat source size (die size), increase
the heat sink volume with larger fans and use of copper base heat sinks. Other parameters (i.e. fin conductivity) have secondary importance.

Figure 4 – (a) Angled Fin Dense Plates and (b) Heat Pipe Remote Cooling

Figure 5– Air Cooling Building Block - Technology Performance

Based on the design of experiments presented in Figure 3 a few reference samples have been fabricated. Figure 4 shows the photos of two technologies which extend air cooling: the “Angle Fin Dense Plates” and the conventional “Heat Pipe Remote Cooling”. Figure 5 shows a summary of the cooling performance for these technology options. It can be seen that simple technologies ranging from high fin density to heat pipes with large remote heat sinks could potentially decrease the sink to ambient thermal resistance to about 0.18 °C/W for Architecture II Products. The constraints encountered in microprocessor cooling have been taken into consideration and more details are obtainable from Sauciuc et. al [10;11]. These studies showed that air cooling improvements present diminishing returns and other technologies should be the focus of the research and development.

High Thermal Conductivity Materials

Significant improvements in heat sink performance may be realized if high conductivity materials are used for the heat sink base. Unfortunately, the conventional materials with very high conductivity (i.e. diamond) are very expensive. Some anisotropic materials (i.e. graphite) have been proposed in the last years.

Figure 6 - Particular Study - Anisotropic Materials Effect on Sink to Ambient Resistance

Figure 6 presents the results of a study of anisotropic materials. The materials proposed for this investigation have a very high in-plane thermal conductivity (x and z directions), with a low thermal conductivity in the normal direction (y). Graphite is one example of a material with this property. For this particular study, the normal thermal conductivity (ky) was varied between 50 W/mK to 360 W/mK. The anisotropic heat sink (80mm x 80 mm x 60 mm) was compared with a heat sink made of copper for an Architecture II type test vehicle. Both heat sinks have same geometry and are using same fan and more details are presented in [2;10;11]. It can be seen that, for significant improvements, ky should as high as possible, even for high in-plane conductivities. To the best knowledge of the authors, current anisotropic materials have normal conductivities less than 100W/mK. Therefore, more research needs to be done in this area, to increase ky in values larger than copper’s conductivity. In addition, these materials tend to be cost prohibitive for the electronics cooling market. Therefore, it can be concluded that so far it is very difficult to find cost-effective materials to improve the spreading resistance of the heat sink base. This is a key challenge for this building block. However we did not determine if there are particular geometries where it make sense to use the current anisotropic materials.

Passive Phase Change (liquid/vapor) Spreaders

Another way to improve spreading is by using two-phase (liquid/vapor) devices. Despite many experimental and theoretical studies in heat pipes, vapor chambers and thermo siphons [10;13;21-37], it is arguable that the fundamental theory in heat pipes and vapor is well behind the experimental work, mainly in explaining heat transfer phenomena in the wick structure and in the evaporator section. Therefore most of the heat pipe/vapor chamber/thermosiphon designs are based on empirical experimental data and “know how” of each heat pipe/vapor chamber manufacturer.

Due to the large amount of work in boiling/phase change over the last decades we defined the reasonable phase change limit
based on experimental data only. Although some references [38] suggest the possibility of achieving heat transfer coefficients in excess of 100,000 W/m²K none of our testing could confirm this in case of Architecture II test vehicles. Other parameters such as heat carrying capacity and the burnout flux are not discussed here since the first objective is to reduce thermal resistance.

Figure 7. Schematic of the evaporator section for a thermosiphon

The most used metrics in phase change devices is the evaporator resistance as defined in equation (3) (which is the major contributor to the total resistance of the phase change device). The location of the sink and adiabatic temperatures are shown in Figure 7.

\[
\theta_{\text{Evap}} \approx \frac{T_s - T_{\text{ad}}}{TDP} \quad (3)
\]

Figure 8. Photos of the (a) Conventional Uniformed Porous Layer (UPL) (b) Sintered structures SEM Photos of the Micro Porous Layer (MPL) boiling structures

Several types of optimized boiling structures were tested using Architecture II type test vehicles. Figure 8(a) shows the conventional sintered boiling surfaces and figure 8(b) shows more developed MPL surfaces [44]. The comparison data is presented in figure 9 which also include other types of boiling surfaces: sintered (A&B types) and wire mesh (water was used as working fluid for all type of experiments). The ambient temperature for all tests was room temperature of about 23-25 °C nad this may translate in operating vapor temperatures of about 35-45 °C.

Figure 9. Thermosyphon test data with different boiling/phase change surfaces using Architecture II with 120W

The evaporator resistance was determined at a horizontal orientation for the boiling surface. It can be seen that the evaporator resistance for most of the surfaces was about 0.1 °C/W using Architecture II Test Vehicles and we consider this to be the practical performance extension for the phase change devices. Also, we would like to emphasize that experiments must be done in order to establish the evaporator performance for each particular application and other parameters such as heat carrying capacity and the burnout flux should also be considered.

TEC Based Cooling Devices (enabling)

Another technology to be discussed is a cooling apparatus with no moving parts using conventional TEC combined with conventional spreading devices (Vapor Chamber, Thermosiphon or Heat Pipe). Figure 10 shows the integration of TEC with other components.
Figure 10. TEC Based Concept Thermal Solution

The spreading device conducts the heat to the cold side of a conventional thermoelectric device. Several TEC modules are used to introduce a negative (effective) resistance into the chain of thermal resistances, thus decreasing the operating temperature of the spreading device.

One measure of performance of a TEC is the COP (coefficient of performance). It is the ratio of two heat flow terms as give by equation (4):

$$COP = \frac{Q_{CPU}}{P_{TEC}}$$  \hspace{1cm} (4)

Figure 11 presents the model and test data showing the thermal capability for a remote 40 mm tall heat sink using TEC based thermal solution using heat pipes for spreading. The analytical model is based on the estimation of individual component thermal performance (i.e. spreading, fins resistance, etc.) and than integrated into one dimensional analytical model. These details have been already discussed by Sauciuc et. al [12;13]. The horizontal line at just over 0.18 °C/W thermal resistance without the TECs represents the conventional parallel plate air cooled heat sink (see Air Side Cooling Building Block). It can be seen from this figure that significant thermal improvements over conventional air cooling can be obtained even at 160 W and COP=3. For the case studied here, the thermal improvement (reduction in effective heat sink resistance) for this solution range from about 0.06 °C/W to 0.11 °C/W for IHS type processors. This graph also shows a single data point, represented by the yellow diamond, which is the measured mean of 20 samples. This measurement reconfirms the TEC capability and model prediction. The key challenges for this building block are cost reductions, improved reliability and improved thermoelectric materials.

Thermal Interface Building (Block)

The thermal interface material (TIM) performance and the bond line thickness (BLT) is usually measured in an ASTM-based [40] material tester [Figure 12]. Other researchers [41;42;43] have already presented different thermal interface materials but how significant are the overall junction to ambient improvements was not addressed.

Figure 12: ASTM-based Material Tester

The above method is used by many TIM manufacturers to estimate the performance of TIM and to develop new formulations of TIMs. Some advantages of the material tester include the controlled co-planarity between surface of interest,
the ability to measure the TIM thickness, the ability to apply an accurate pressure on the TIM, and a controlled uniform temperature at the TIM-surface interface.

Table 1: TIM performance data from Material Tester measured at 0.621 MPa loading on TIM

<table>
<thead>
<tr>
<th>Material</th>
<th>θ_{TIM} (°C-cm²/W)</th>
<th>BLT (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grease 1</td>
<td>0.02</td>
<td>7.6</td>
</tr>
<tr>
<td>Grease 2</td>
<td>0.06</td>
<td>17.8</td>
</tr>
<tr>
<td>Grease 3</td>
<td>0.16</td>
<td>7.6</td>
</tr>
<tr>
<td>Gel 1</td>
<td>0.05</td>
<td>7.6</td>
</tr>
<tr>
<td>*PCM 1</td>
<td>0.08</td>
<td>27.9</td>
</tr>
<tr>
<td>*PCM 2</td>
<td>0.11</td>
<td>48.3</td>
</tr>
<tr>
<td>*PCM 3</td>
<td>0.11</td>
<td>7.6</td>
</tr>
<tr>
<td>*PCM 4</td>
<td>0.18</td>
<td>101.6</td>
</tr>
<tr>
<td>Foil 1</td>
<td>0.16</td>
<td>50.8</td>
</tr>
<tr>
<td>Foil 2</td>
<td>0.11</td>
<td>10.2</td>
</tr>
<tr>
<td>Solder 1</td>
<td>0.11</td>
<td>127</td>
</tr>
<tr>
<td>Solder 2</td>
<td>0.18</td>
<td>127</td>
</tr>
</tbody>
</table>

*PCM: Phase Change Material

Table 1 shows the TIM performance and BLT measured in an ASTM-based material tester. The test data range from 0.02 °C-cm²/W to 0.2 °C-cm²/W. This table shows that the thermal performance of TIMs can be pushed to very low levels so any more future improvements will bring diminishing returns. One factor to focus for the industry: the thermal interfaces can degrade with usage. Degradation in TIM performance depends on usage temperature, the time of usage, mechanical loading, and material properties. Since all factors are not well understood, TIM degradation should be characterized using empirical methods.

Micro channel Cooling Building Block (package)

Various innovative designs on the use of micro channel heat sinks for CPU cooling applications have appeared during the past decade, as dramatic improvement in the techniques of micro fabrication has made the technology more feasible. Current priority is to develop a single-phase cooling system, as the technology is more mature in the industry. For the package based technologies (Architecture I- Figure 1) we propose to have a micro channel cold plate in contact with the back-side of the die. The cold plate design includes a set of parallel micro channels with a width from tens to hundreds of microns. These micro channels provide extended surface area for heat transfer to the coolant. Due to their extremely small hydrodynamic diameter the cooling performance is very good. The micro channel packaged heat sink was is based on the concept that the micro channels provide high surface area to volume ratios and also serve to enhance the heat transfer coefficient significantly in the laminar flow regime where heat transfer coefficient is inversely proportional to hydrodynamic diameter. As a rule of thumb, all channels with characteristic dimensions between 1 µm and 1 mm are typically called micro channels. Figure 12 shows the micro channel cold plate combined with a pump and a remote heat exchanger.

Figure 12. Schematic of the Micro-Channel Cooling System (Architecture I)

The thermal resistance of a micro-channel cooling system is defined in equation 5 below. The model prediction of the thermal capability for the micro channel cold plate is plotted in Figure 13 for different selected fluid viscosities. It can be seen that within reasonable pressure drop for the pump, the junction to inlet resistance can be decreased to about 0.1 °C/W which is considered a practical limit for a 10 mm x 10 mm test die (commercial available CFD model for a single phase fluid).

\[
R_{j-inlet} = \frac{T_{j,max} - T_{fluid,in}}{T_{DP}}
\] (5)
The test data for optimized single phase liquid cooling (LC) using Propylene Glycol as working fluid and a two-phase forced convection (2PFCC) using some refrigerant is presented in Figure 14. It can be seen that these particular optimized single phase has a smaller resistance at lower TDP but the two-phase devices are becoming better at larger TDPs. The fact that the two-phase resistance is lower at larger TDP is explained by the fact that boiling improves with the increase in the heat flux.

**Figure 13. Extension of the micro channel resistance vs. pressure drop**

The key challenge for micro channel development is to develop a pump which uses the working fluid as lubricant for the bearing. Most likely water cannot be used as a coolant due to freezing issues whereas traditional antifreeze coolants such as Propylene Glycol (50%) have very high viscosity and low thermal conductivity (50% of water). Therefore, there is also a need to develop alternate antifreeze coolants.

**Single Phase/ Two Phase Active (enabling)**

Except for TEC based devices all future enabling cooling technologies may require some fluid moving device (i.e, pump or compressors). Most of the current development for active devices is focused on single phase liquid cooling, two-phase liquid cooling and vapor compression refrigeration.

The definition of the cold plate resistance is similar to the microchannel cold plate resistance with the only change is substituting the $T_j$ with $T_s$, for simplicity we considered:

$$\theta_{cp} = \frac{T_s - T_{in}}{TDP} \quad (6)$$

**Figure 14. Typical Cold Plate Resistance Variation for Architecture II at 120W heat load**

Key Challenges for the micro channel is to develop a long life bearing.

**Refrigeration Building Block (enabling)**

A compact miniature compressor system that uses R-134a as a refrigerant, may be the ultimate method for cooling high power density electronic components. Brown at al. [20] shows the performance of such a refrigeration system developed together with Intel Corporation [Figure 15].

**Figure 15 Proposed refrigeration system (Courtesy of Kryotech)**

Figure 15 shows the proposed refrigeration system. The system has the same basic components as a standard vapor-compression system; compressor, evaporator, condenser and expansion valve, but are using a new rotary compressor measuring 3.5 inches high and 2.5 inches in diameter. The entire refrigeration system measures 16 inches long, 7 inches wide and 3.5 inches high.
Figure 16. Refrigeration Performance

Figure 16 shows COP and $\theta_{sa}$ data as the condenser cooling fan speed (air flow rate) is varied. The data shows a gradual decrease in $\theta_{sa}$ with increased condenser fan speed on the order of 11%. The cold plate temperature (evaporator) decreases slightly and then holds a relatively constant value around 11°C. The system COP is shown to decrease slightly with increasing condenser fan speed. This is a result of increasing compressor operating temperature for this testing scenario.

Figure 17 COP versus evaporating temperature for R-134a at condensing temperature of 45°C and constant cooling capacity of 100 W

Trutassanawin et al. [45] presented a detailed study to investigate the thermal resistance capability at high evaporating temperatures. As expected, the COP of the system increases with an increase of the evaporating temperature as shown in Figure 17 and approaches infinity at the limit of an evaporation temperature of 45°C, in which case the evaporation temperature is equal to the condensation temperature. At this, no mechanical power is needed to run the system and the system would operate as a heat pipe. This shows that there may be very significant benefits for having refrigeration systems at high evaporator temperatures. The key challenges for this building block are: cost, bearing reliability and operation at all orientations. Although refrigeration may look promising as an option, the maturity of development on low compressor size, operation at all orientations, water condensation and cost are major high risks items. This leaves micro channel based technologies as one of the future major focus packaged based technology.

Summary - Future Technology Focus and Challenges

Based on the DF$_j$, defined at the beginning of this paper and using the data from each building block the proposed technologies are compared against conventional air cooling (Figure 18).

\[
\text{Cooling Limit Improvements} = \frac{\Psi_{j\text{technology}} - \Psi_{j\text{air cooling}}}{\Psi_{j\text{air cooling}}} \quad (7)
\]

It can be seen that at low DFs the enabling technologies provide significant improvements, however as the DF increases the difference between technologies is not so significant with the microchannel equaling the enabling refrigeration (theta$_{sa}$ for refrigeration is $\Psi_{sa} = 0$ °C/W in order to avoid condensation). There are key high risk concerns associated with all of the future technologies since most of them are using rotation devices which need to ensure high package reliability. The low size of the devices imposes significant larger forces on bearings reducing the lifetime of the pumps.
only consider that approximately 0.08-0.1 oC/W. For the TEC based passive using a range of “reasonable” boundary conditions. Model and for future enabling and package based cooling technologies quantify thermal performance and determine the key challenges.

Conclusions

18 and Table 1.

concepts and to make the necessary cost tradeoffs using Figure

not applicable for all market segments (i.e. mobility). The

refrigeration does not work at all orientations which makes it

significant challenge for all of these technologies. In addition,

(rotating device) thus the bearing reliability may be the most

proposed and the key concerns associated with it. It can be seen

cooling technologies

10 Copyright © #### by ASME

References


Table 2. Qualitative comparison for different future CPU cooling technologies

Table 2 presents a comparison of different technologies proposed and the key concerns associated with it. It can be seen that most of the promising technologies are using some active (rotating device) thus the bearing reliability may be the most significant challenge for all of these technologies. In addition, refrigeration does not work at all orientations which makes it not applicable for all market segments (i.e. mobility). The designer has the challenge of integration of the proposed concepts and to make the necessary cost tradeoffs using Figure

18 and Table 1.

Conclusions

This paper addresses uses a “building block” approach to quantify thermal performance and determine the key challenges for future enabling and package based cooling technologies using a range of “reasonable” boundary conditions. Model and test data shows that the thermal resistances of the cold plates for both liquid cooling and phase-change device can drop to approximately 0.08-0.1 °C/W. For the TEC based passive devices values lower than Ψsa =0.1 °C/W for powers up to 120-130 Watts at a high coefficient of performance (COP=3) can be obtained. The enabled vapor compression refrigeration cooling test data shows that the thermal resistances of the entire system can be negative and can drop to approximately Ψsa = -0.1 °C/W, but, in order to avoid condensation, for this study we only consider that Ψsa down to 0 °C/W. Using reasonable boundary conditions for the micro channel cooling, we have shown more than 100% improvements at low non-uniformity heating and more than 50% at high non-uniformity heating compared to conventional air cooling. For particular sets of reasonable boundary conditions and hot spot density factor, the cooling capability of different technologies may significantly increase if the industry and academia will further focus and solve the key challenges presented in the paper.

References


